METHOD TO REDUCE TRANSISTOR CHANNEL LENGTH USING SDOX

ABSTRACT

An improved method of reducing transistor channel length is shown. The physical channel length is reduced below a length set by the minimum lithographic feature size by implanting source/drain region extensions. The physical gate width is then narrowed by oxidizing the walls of the gate. The combination of narrowing the physical channel length and narrowing the physical gate width results in an effective channel length L_{eff} that is more narrow than possible using lithography alone. The negative side effects of increasing effective gate thickness are eliminated through the use of a barrier layer.